

FIG. 1a
(PRIOR ART)

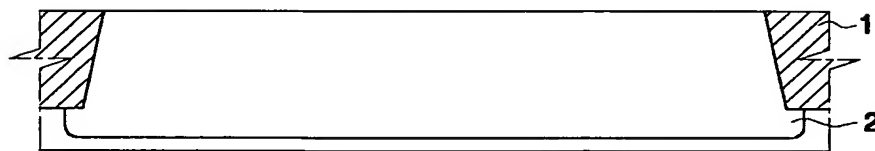


FIG. 1b
(PRIOR ART)

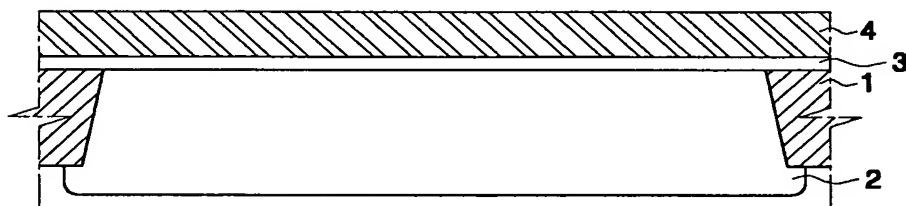


FIG. 1c
(PRIOR ART)

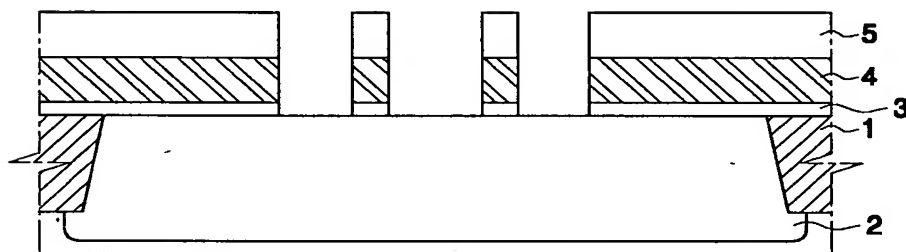


FIG. 1d
(PRIOR ART)

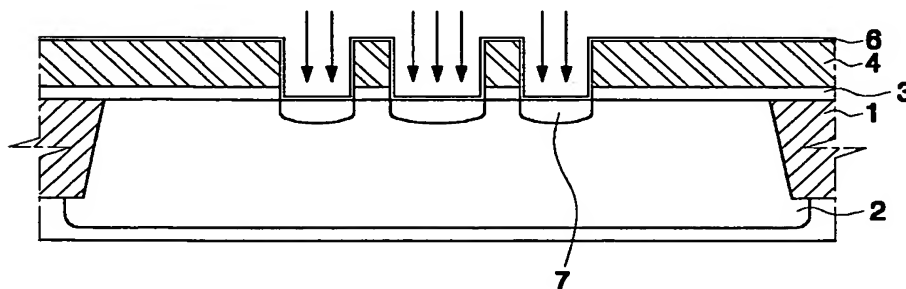


FIG. 1e
(PRIOR ART)

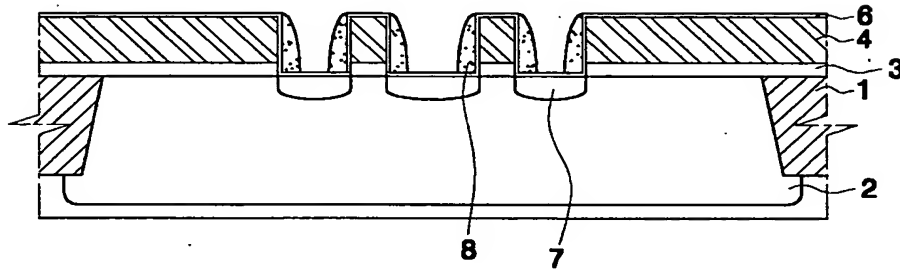


FIG. 1f
(PRIOR ART)

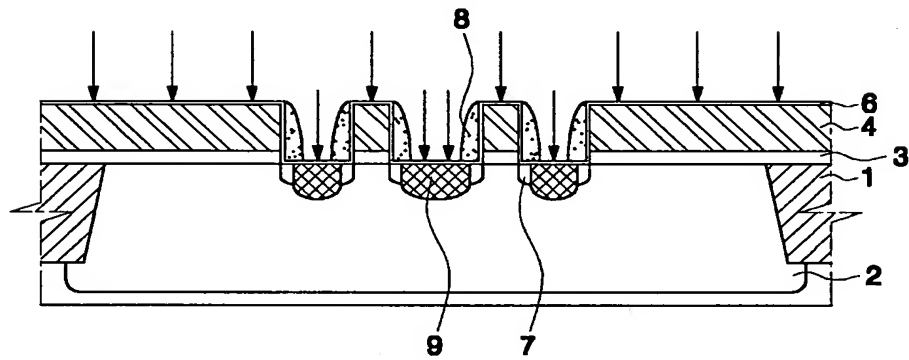


FIG. 1g
(PRIOR ART)

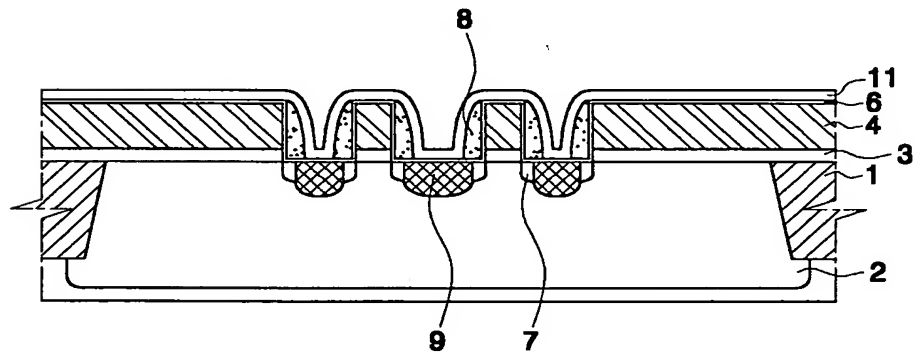


FIG. 1h
 (PRIOR ART)

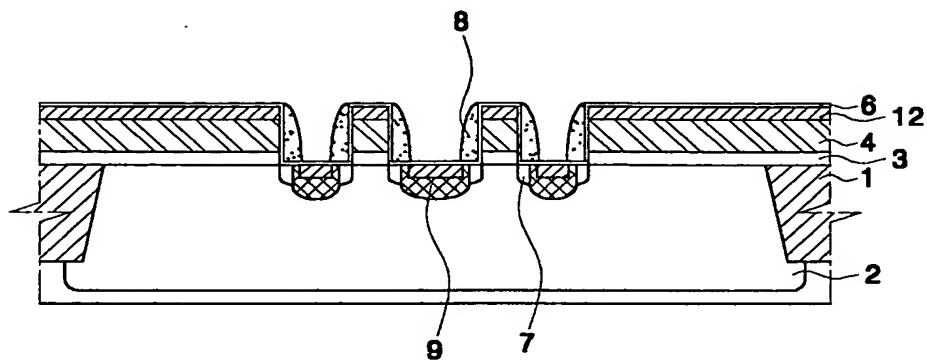


FIG. 1i
 (PRIOR ART)

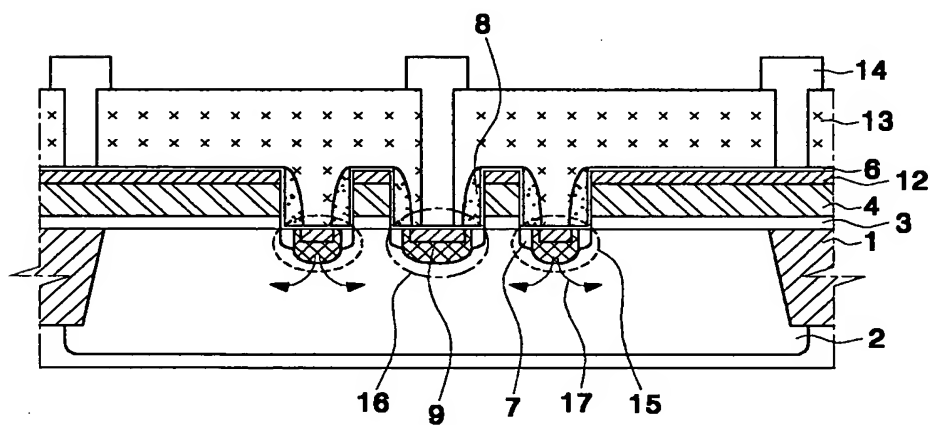


FIG. 2a

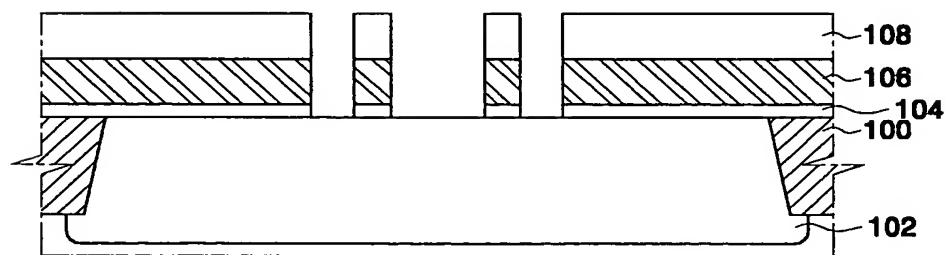


FIG. 2b

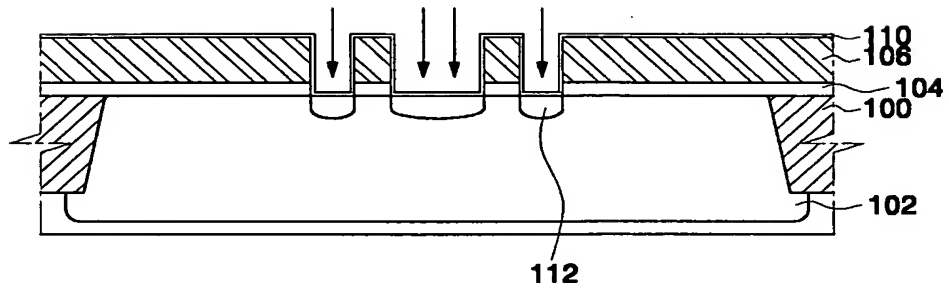


FIG. 2c

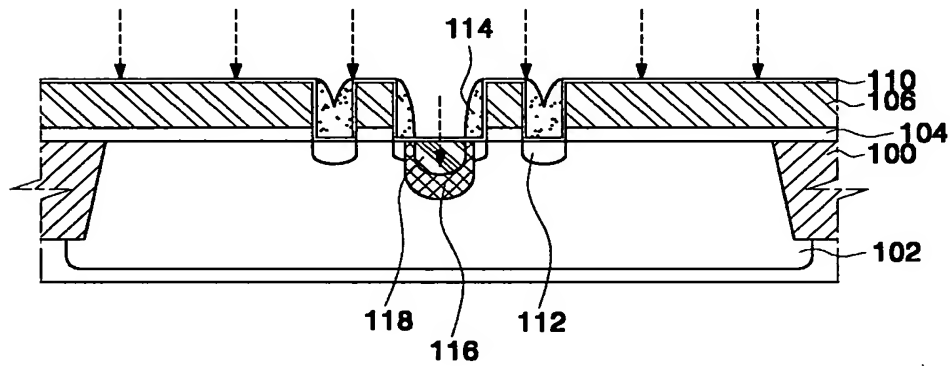


FIG. 2d

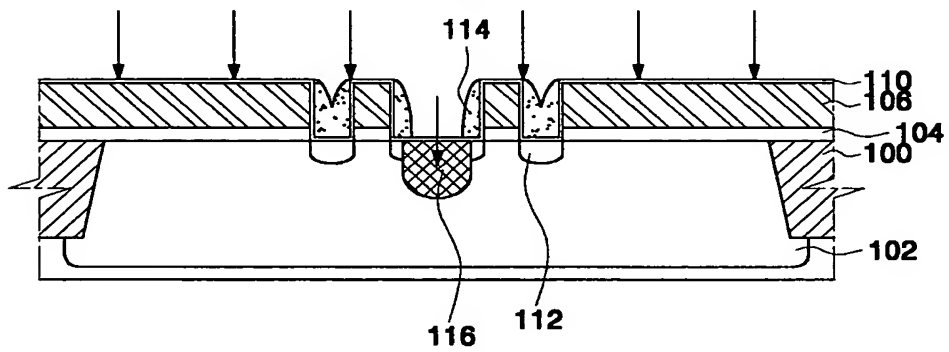


FIG. 2e

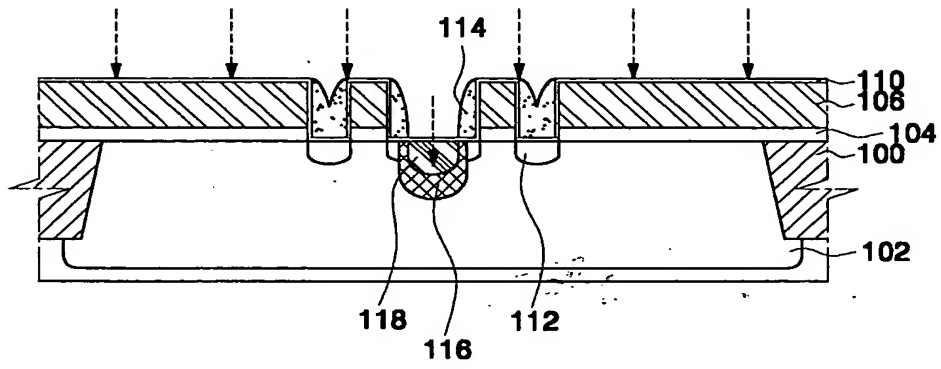


FIG. 2f

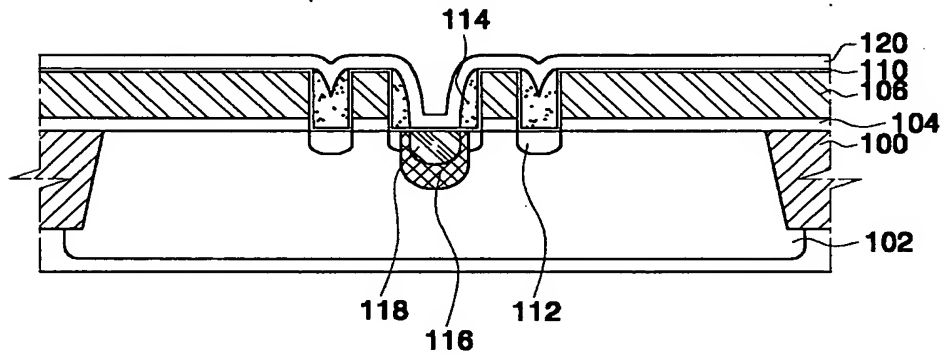
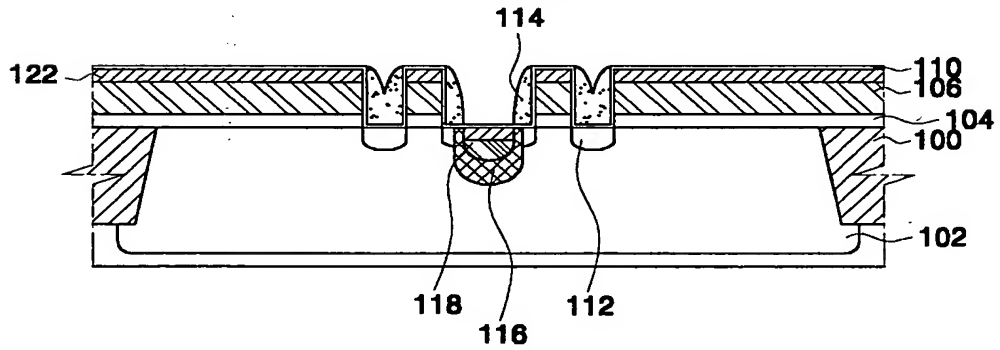


FIG. 2g



This cross-sectional view shows a semiconductor device with a central gate structure. The gate stack includes a gate dielectric layer (114) and a gate conductive layer (110). The gate conductive layer is patterned into a central gate (116) and side gates (112, 118). The side gates are connected to a common source/drain contact (104) which is formed in a conductive layer (106). The device is surrounded by a substrate (100) and a passivation layer (102). The top surface is covered by a protective layer (122) with a pattern of cross-hatches. The side walls of the gate stack are labeled 124 and 126. The bottom of the device is labeled 128.

A cross-sectional view of a substrate assembly. It consists of a top layer (110) with diagonal hatching, a middle layer (108), and a bottom layer (100) with diagonal hatching. A central cavity (102) is formed in the bottom layer. Three downward-pointing arrows are shown within the middle layer, indicating a process step. A wavy line (113) is shown at the bottom of the cavity. The top surface of the middle layer is labeled 104.

FIG. 3c

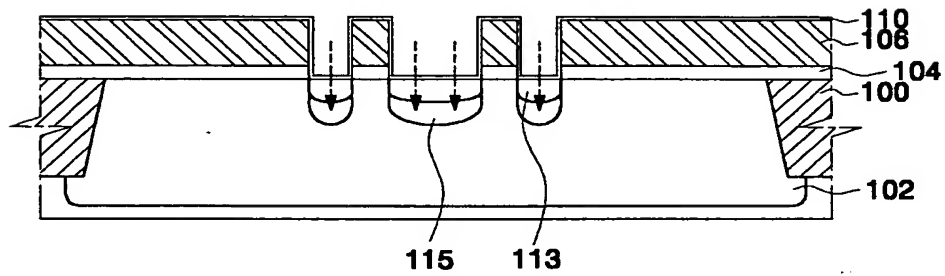


FIG. 3d

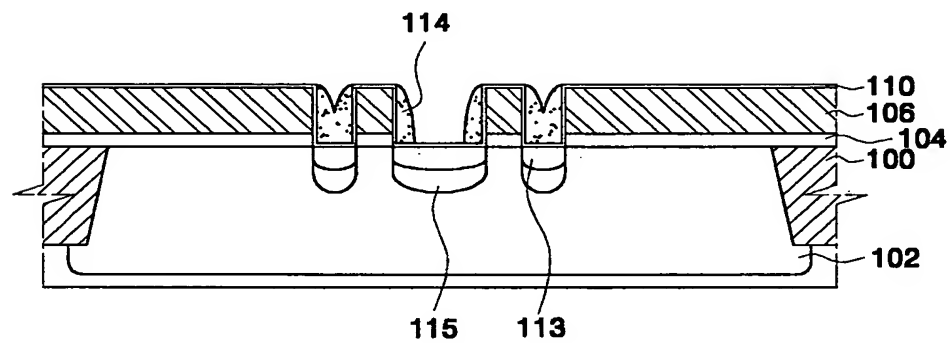


FIG. 3e

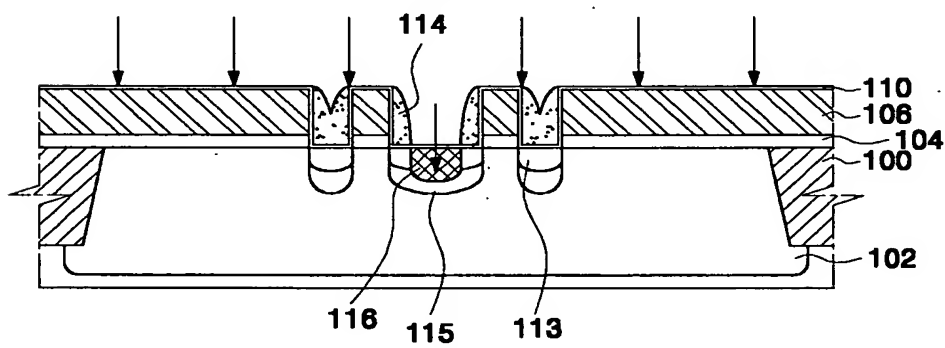


FIG. 3f

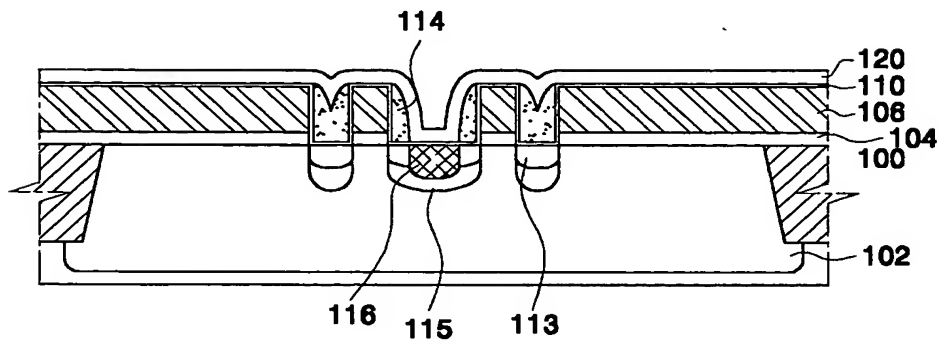


FIG. 3g

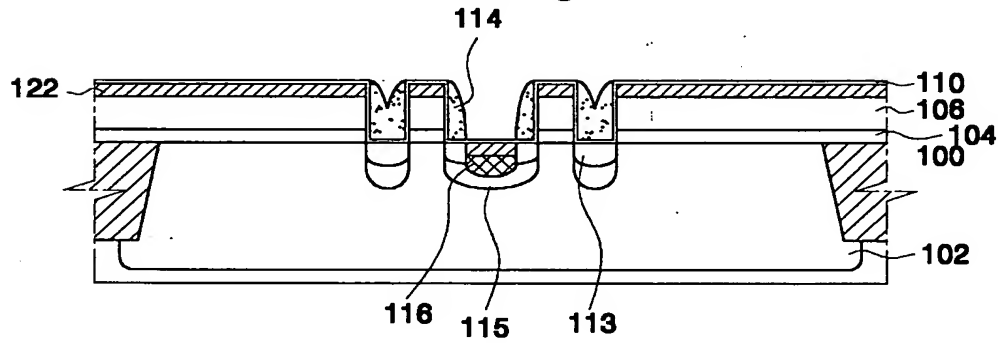


FIG. 3h

